Self-Aligned Silicon Interposer Tiles and Silicon Bridges Using Positive Self-Alignment Structures and Rematable Mechanically Flexible Interconnects

Hyung Suk Yang, *Student Member, IEEE*, Chaoqi Zhang, *Student Member, IEEE*, and Muhannad S. Bakir, *Senior Member, IEEE*

***Abstract*— A novel large-scale silicon system platform is proposed and demonstrated. In this paper, three silicon interposer tiles are aligned and mounted on a printed wiring board (PWB), and two silicon bridges are aligned and mounted on top of the three interposer tiles; each silicon bridge spans two interposer tiles. Four positive self-alignment structures and four inverted pyramid pits self-align a tile to the PWB and a bridge to two tiles. Mechanically flexible interconnects (MFI) form nonbonding electrical connections between the three interposer tiles and two silicon bridges; MFIs are fabricated on the interposer tiles. Pointy tips on the MFIs form low contact resistance with the pads on the silicon bridges. Less than 4 μm alignment error is demonstrated on a stack of silicon substrates, and <8 μm alignment error between a silicon bridge and tiles is also demonstrated on a FR4 substrate. Daisy chain and four-point measurements are performed to verify electrical connections between the three interposer tiles via MFIs and silicon bridges.**

***Index Terms*— Electronics packaging, integrated circuit interconnections.**

I. Introduction

THE advent of portable electronic systems and high-performance computing systems, along with the challenges in sustaining performance gains by transistor scaling, have led to the emergence of 2.5-D and 3-D integration platforms as key-enabling technologies for the next generation of microsystems. More specifically, 2.5-D integration, which involves the use of silicon interposers to increase chip-to-chip bandwidth, has received significant interest from both academia and industry, because it provides the benefits of multichip integration without the significant bandwidth limitation caused by the package substrate. To this end, there have been many significant advances in the industry. Most recently, Xilinx demonstrated that silicon interposers could circumvent the yield issues in manufacturing by replacing a single large IC with multiple smaller ICs that are interconnected with high-density wiring on a silicon interposer [1].

However, the interposer-based interconnection is only a partial solution to the rapidly growing chip-to-chip bandwidth requirement, because an interposer size is limited by both technical and economical constraints, and in turn, it ultimately limits the size and the number of chips that can be assembled on top. Eventually, multiple interposers may become necessary, and high-bandwidth interconnections between interposers will become vital in providing a contiguous macrochip as discussed in [2].

To that end, this paper presents and demonstrates a novel large-scale silicon platform consisting of multiple interposer tiles, which are essentially silicon interposers that are assembled directly on the printed wiring board (PWB) (Fig. 1) in a tile-like pattern. Electrical interconnections between the tiles are provided through silicon bridges, which are mounted on top and span two or more interposer tiles. The tiles and the bridges are electrically interconnected using mechanically flexible interconnects (MFIs) with pointy tips, which are developed to allow repeatable and low resistance contact with electrical pads. Positive self-alignment structures (PSASs) and inverted pyramid pits passively self-align the interposer tiles with the FR4 PWB and the interposer tiles with the silicon bridges. This demonstration is a first step toward the goal of a platform that provides high bandwidth and low-energy per bit (EPB) interconnections among interposer tiles. The key features of this demonstration are: 1) accurate alignment of interposer tiles, bridges, and PWB and 2) electrical interconnectivity among tiles through the bridges.

Ultimately, nanophotonics would be integrated into the platform for interconnect lengths that offer better bandwidth density and EPB. Krishnamoorthy *et al.* [2] demonstrated the need for a high chip-to-chip communication bandwidth with improved energy efficiency for large systems, which could not be fulfilled by conventional interconnect and packaging technologies. As a solution, the researchers demonstrated a novel silicon nanophotonic technology that consumed EPB of 300 fJ/bit [3] and integrated receivers with -18.9 dBm sensitivity at 5 Gb/s for a bit error rate (BER) of 10^{-12} [4].

For photonic interconnected systems, however, a very accurate alignment between substrates is required to achieve such

Manuscript received January 31, 2014; revised June 6, 2014; accepted August 6, 2014. Date of publication October 13, 2014; date of current version October 31, 2014. Recommended for publication by Associate Editor J. J. Pan upon evaluation of reviewers' comments.

The authors are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: jyang@gatech.edu; chqzhang@gatech.edu; muhannad.bakir@mirc.gatech.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCPMT.2014.2357020

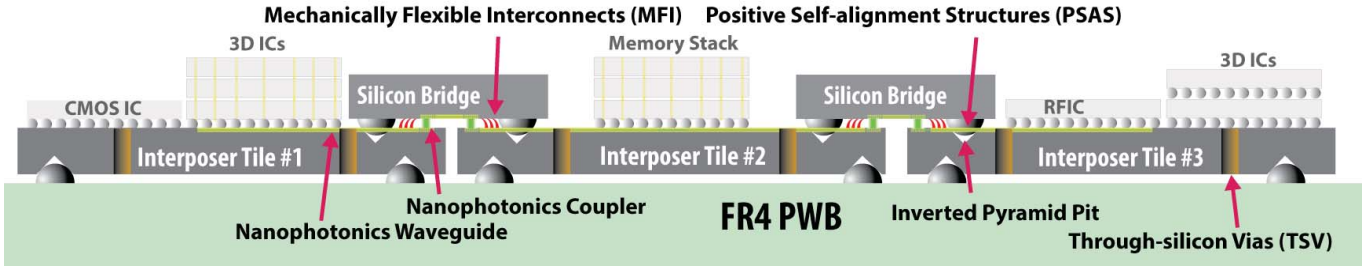

Fig. 1. Direct mounting of silicon interposers on FR4 PWB by using PSASs and MFIs.

performance because the misalignment degrades performance significantly. For example, a nanophotonics system using silicon-based micromirrors requires a submicrometer alignment accuracy to achieve <3 dB of optical loss and a BER below 10^{-12} [5]. Another study that used grating couplers to improve the misalignment tolerance still resulted in 1 dB excess loss for a 2 μm misalignment [6]. Misalignment is also known to negatively impact signal-to-noise ratio of capacitive and inductive coupled interconnects [7]. The need for alignment accuracy is the motivation for PSAS and pits.

Another key feature of the platform is the ability for all tiles and silicon bridges to be replaced individually at any point in time. MFIs, PSAS, and nanophotonics do not require permanent assembly techniques; instead, these technologies only require a vertical clamping force while the system is being used, and the self-alignment mechanism and the interconnects can disengage and reengage just by releasing and reapplying the clamping force.

The two key technologies that are used in this demonstration are: 1) PSAS and inverted pyramid pits and 2) MFIs. In Section II, PSAS is introduced and experiments are performed to verify that PSAS alignment accuracy is adequate on various types of substrates and that it can be used to align multiple substrates in a stack. In Section III, the MFI technology that can be used in conjunction with PSAS is briefly described. Finally in Section IV, the large-scale silicon platform using both the PSAS and the MFI technologies is demonstrated.

II. PSASs and Inverted Pyramid Pits

A. Overview of the Self-Alignment Mechanism

As mentioned in the previous section, an accurate alignment is critical for nanophotonic interconnects to operate efficiently. However, achieving an accurate alignment by using conventional techniques comes at steep manufacturing costs; for example, Panasonic's flip-chip bonder model FCB3, capable of ± 3 μm alignment accuracy, has a speed of 1.8 s/IC, while Panasonic's BM123, capable of ± 50 μm alignment accuracy, has a much higher speed of 0.12 s/IC [8], [9].

In addition, the ability to control the gap between stacked chips plays an important role in improving the coupling efficiency. Specifically, the reduction of the gap in systems with capacitive coupled proximity I/Os results in increased capacitance between the pads, which improves the BER; a 10 μm gap results in a BER of 10^{-9}, and an 11.5 μm gap increases the BER to 10^{-4} [7]. However, the gap cannot be accurately controlled using conventional assembly methods, and there exists a minimum gap that is determined by the size of the features in between, such as solder balls.

The self-alignment technology described in this paper is consistently shown to achieve alignment accuracy of <4 μm while only requiring initial alignment accuracy of 150 μm; the gap can also be controlled. In addition to the accuracy, this capability has the potential to increase the throughput of the assembly process thereby lowering the cost; this is possible because high-speed 150 μm placement tools can be used in place of highly accurate, but slow, flip-chip bonders.

In the simplest configuration, two substrates are aligned using two types of microfabricated structures: PSAS and inverted pyramid pit structures. On one of the substrates, which must be made of silicon, a standard anisotropic silicon etch process is used to create trenches in the shape of inverted pyramids on each of the corners of the substrate. On the second substrate, which can be any planar material, cylindrically patterned structures made of photoresist are precisely reflowed to form an extruding truncated-sphere structures and placed on each of the corners of the substrate. These two substrates are then brought closely together and manually aligned coarsely; as much as 150 μm (radius of the PSAS) of initial misalignment is tolerated. When perpendicular force is applied against the top substrate, the four PSAS are automatically guided toward the center of the inverted pyramid pit structures, thereby aligning the substrates relative to each other.

There are many alternative self-alignment mechanisms that have been published recently. One self-alignment technique uses surface tension of the solder ball itself [10], as well as the surface tension of water [11] and flux [12]. Although these techniques are good alternative self-alignment technologies for applications that require the use of solder interconnections, complexities are introduced to ensure that the accurate alignment is achieved consistently; clean dicing, chip leveling, and precise volume control are some examples of the factors that must be carefully controlled. In addition, compared with these technologies, the combination of a positive structure and negative structure used in this paper allows one to minimize (as close to 0) the gap between the substrates, which is essential for low-loss nanophotonics interconnected systems.

B. Geometrical Considerations

The shape of the PSAS and the pit structures determine the final relative position of the two substrates. Pit structures have

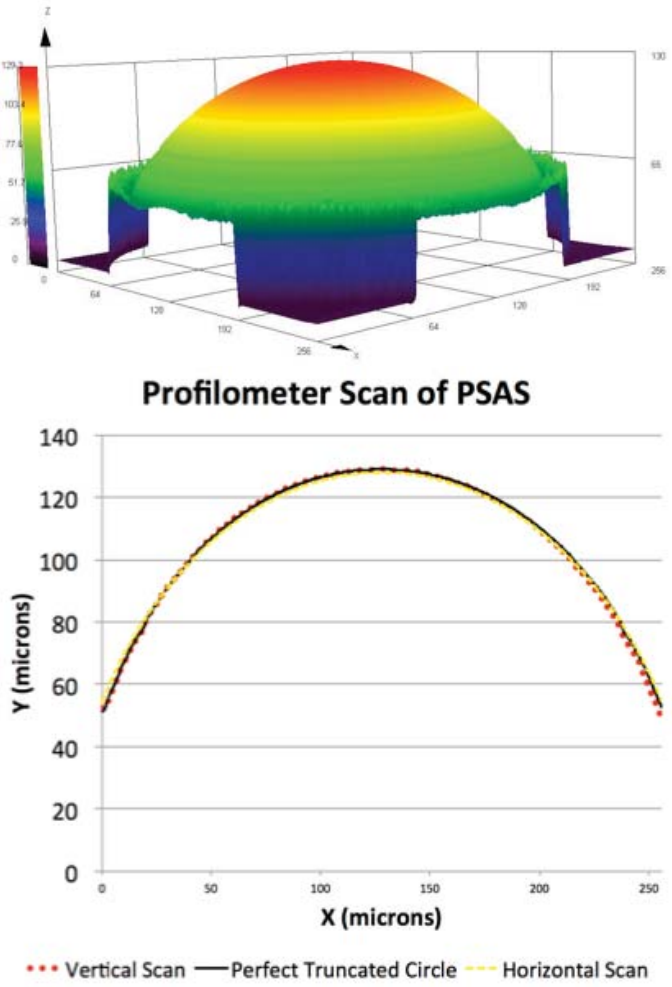

Fig. 2. 3-D image of PSAS scanned by a confocal laser microscope (top), and a plot showing the measured profile of the PSAS through the center point. Also plotted is a perfect truncated circle with a radius of 148 μm. Edges of the PSAS could not be scanned because of extreme tangential angles.

been widely used in the field of MEMS. Moreover, the resulting shape can be predicted accurately. Therefore, in this section, only the shape of the PSAS is determined.

PSAS is fabricated by reflowing a cylindrical structure formed by patterning a thick layer of photoresist. Consequently, the final shape can be determined using the same methods used to predict the shape of a reflowed solder ball; various methods for predicting reflowed solder ball shape have been described in [13].

In this paper, the reflowed structure is approximated as a truncated sphere, which neglects the effect of gravity. To verify that the approximation is accurate in describing the PSAS structure, the shape of the PSAS is measured using a confocal laser microscope; the confocal laser microscope is capable of capturing the profile of a 3-D structure. The captured profile of the PSAS is shown in Fig. 2. The analysis of the captured data shows that:

1) the profile of the PSAS surface through the center can be accurately approximated as a circular segment;
2) the PSAS surface is radially symmetric, evident from the identical horizontal and vertical profiles extracted from the captured data.

From these results, it is possible to conclude that it is reasonable to approximate the shape of PSAS as a truncated sphere.

C. Fabrication of PSAS and Inverted-Pyramid Pit Structures

The alignment accuracy is strongly dependent on the ability to consistently fabricate PSAS and pit as close to the design as possible. Therefore, it is important to control the resulting dimensions of the PSAS and the pit very precisely.

1) Precision Reflow Process: The PSAS is fabricated by reflowing photoresist, which is a technique commonly used to make microlens arrays. Although there are thickness variations inherent to the photoresist reflow process, such variation translates to the variation in the final PSAS shape. However, with the reflow control technique described below, such volume change minimally affects the lateral alignment accuracy, because the center of the PSAS, despite the volume variation, remains the same.

To completely reflow a large photoresist structure, such as PSAS, the reflow temperature must be high. This is because the time in which the photoresist structure remains glassy at an elevated temperature is limited because of the increase in the glass-transition temperature during the reflow process [14]; at low temperatures, the glass transition temperature is raised above the reflow temperature before the photoresist is completely reflowed. However, reflowing at a high temperature causes the photoresist to spread beyond the original pattern and results in a shape that is vastly different from the intended design. To this end, Yang and Bakir [14] have shown that by using temperature ramping even large structures can be reflowed completely without spreading. The same techniques have been used in this paper.

To form PSAS, AZ 40XT-11D from AZ Electronic Materials is first spin coated and then patterned to form a cylinder. Next, using the precise reflow process described previously, PSAS are formed (Fig. 3). A cylinder with a height of 80 μm and a diameter of 300 μm forms a truncated PSAS with a height of 130 μm and a diameter of 300 μm. Cylinder height of 95 μm forms semisphere PSAS with a diameter of 300 μm.

2) Inverted Pyramid Pit Structures: Inverted pyramid pits are fabricated using a chemical wet etch process commonly used to make bulk micromachined devices (Fig. 3). A solution of KOH was used to anisotropically etch the [100] silicon wafer. For CMOS compatibility, TMAH-based etch solution can be used [15]. In calculating the widths of the final pit structure, it is important to note that {111} is also etched, albeit much slower. As a result, the initial opening with a 300 μm $\times$ 300 μm pattern becomes 305 μm $\times$ 305 μm.

D. Substrate Thickness and PSAS/Pit Size

Currently, the die thickness is limited by the height of the PSAS and the expected gap between the substrate. These two factors determine the fraction of the PSAS volume that is completely inside a pit, which directly determines the minimum depth of the pit that is required. For the dimensions

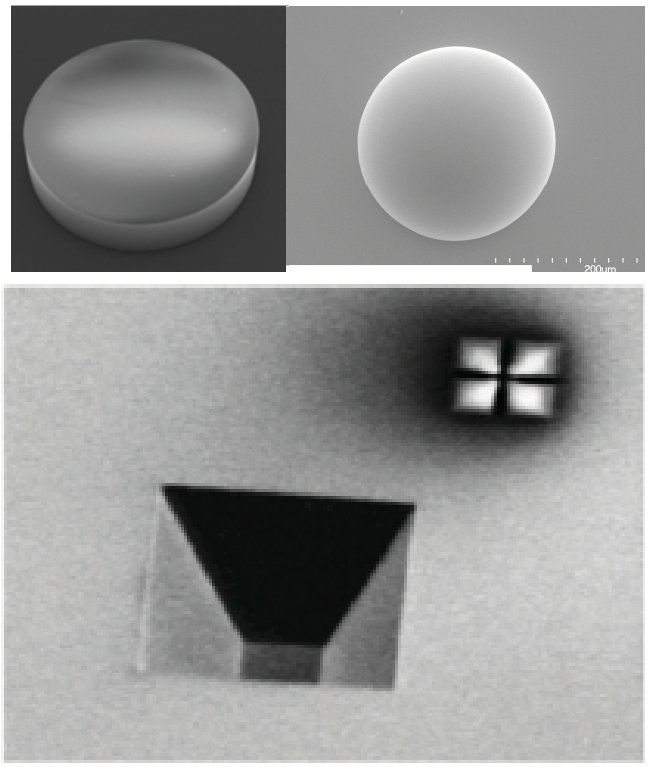

Fig. 3. SEM images of a PSAS, before (left) and after (right) the reflow, and an inverted pyramid pit structure.

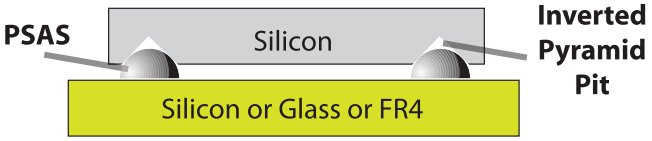

Fig. 4. Silicon substrate with four inverted pyramid pits are aligned with three different types of substrates containing four PSAS on the surface.

of the PSAS chosen for this paper, the minimum thickness of the interposer is approximately 150 μm.

However, it is possible to use smaller PSAS to enable the use of thinner dice, for example, PSAS with 50 μm radiuses. The tradeoff in such situation is that initial misalignment must be within 50 μm.

E. Misalignment Measurement Setup

Vernier patterns are used to measure misalignments. The patterns include two separate scales that are aligned in the center, but have a different spacing between tick marks; when two scales become misaligned relative to each other, the center tick marks become misaligned. However, because of the different spacings between the two scales, another set of tick marks, away from the center, becomes aligned instead. By determining which of the tick marks are aligned, and the location of such tick marks relative to the center, it becomes possible to measure the misalignment with a resolution that is significantly smaller than the tick mark spacing.

F. Alignment Results

Two capabilities of PSAS-based alignment must be demonstrated to enable the configuration as shown in Fig. 1.

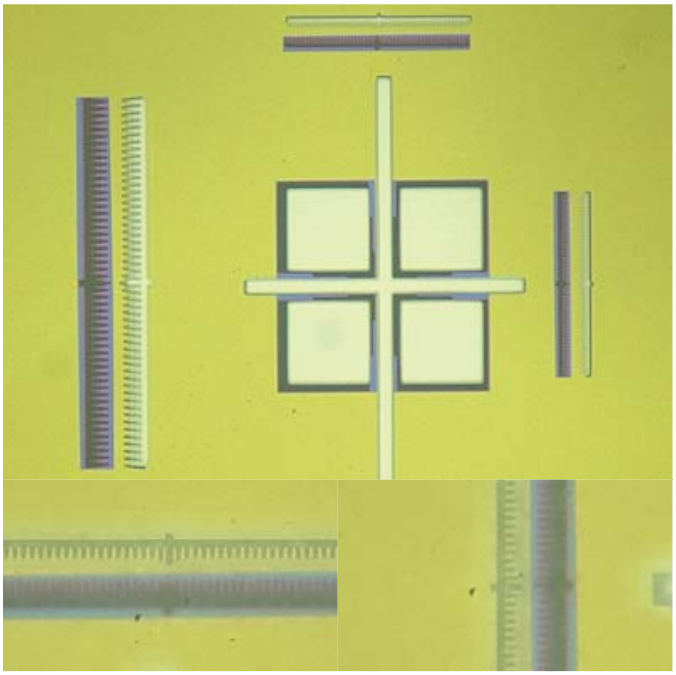

Fig. 5. Optical microscope images showing the overlay of two vernier scale patterns. Bottom images show high-magnification images of the smallest vernier patterns.

TABLE I
MISALIGNMENT IN μm FOR SILICON-TO-SILICON/GLASS/FR4 SUBSTRATES

Regions	Glass		Polished Silicon		FR4	
	X	Y	X	Y	X	Y
	(μm)		(μm)		(μm)	
Bottom Left	>-1	+1	<+1	<+1	+4.4	+2.0
Bottom Right	-1	<+1	+1	+1	+3.2	-3.2
Top Right	+1	-5.8	<+1	+1	-1.6	-3.2
Top Left	+1	-5.6	<+1	<+1	-2.8	+2.4

The first capability is the ability to align a silicon substrate with a substrate made of silicon, glass, and FR4. This would demonstrate that the PSAS can be used to align silicon-based interposer tiles directly on an FR4 package substrate. The second capability is the ability to align multiple substrates on top of each other. This is important because the PSAS is used to align a stack of three substrates in the proposed platform.

1) Aligning Silicon Chip With a Silicon Substrate, a Glass Substrate, and an FR4 Substrate: In this experiment, four inverted pyramid pits are fabricated on a 2 cm $\times$ 2 cm silicon substrate, whereas four PSAS are fabricated on three different types of substrates: silicon, glass, and FR4 (Fig. 4). The alignment is performed manually using PSAS and without an aid of a placement tool; the alignment accuracy is measured by visually observing the vernier patterns using an infrared (Fig. 6) or an optical (Fig. 5) microscope. Table I shows the results of the experiment.

To observe smaller vernier patterns, which can resolve much smaller misalignments, higher magnifications were needed on the infrared microscope. However, because of the gap between

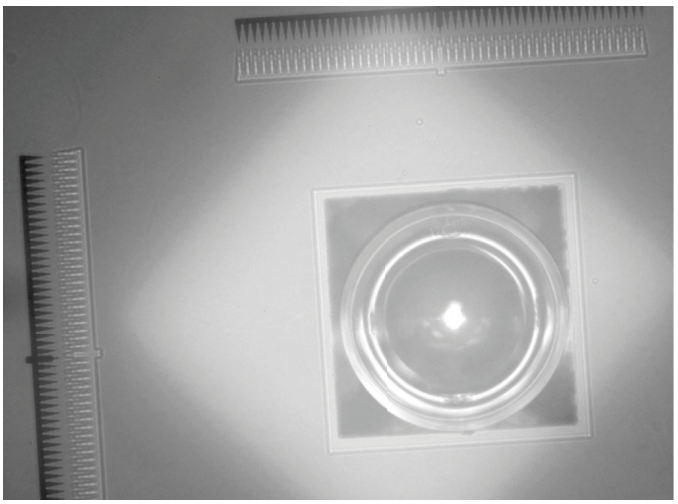

Fig. 6. Infrared microscope image showing a PSAS inside the pit.

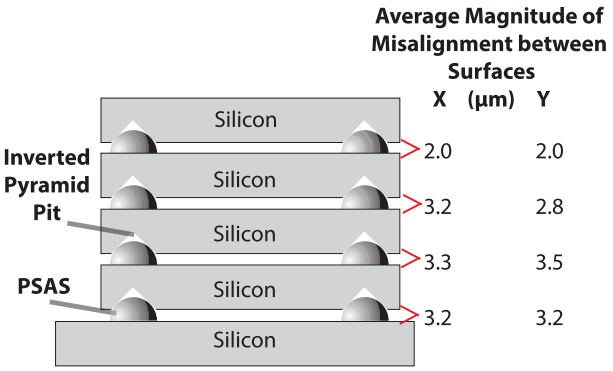

Fig. 7. Five silicon substrates are aligned and stacked on top of each other. The average magnitude of misalignment at each interface is shown.

two aligned surfaces, this made simultaneous focusing of the vernier patterns on the two surfaces impossible. To remedy this, two sets of microscope images were captured each with a different focal plane; images were merged in the postprocessing similar to the focus stacking technique.

For aligning two silicon substrates, the measured misalignment was within or equal to the accuracy of the mask used (1 μm). For glass substrates, the measured misalignment was within the accuracy of the mask used except in the y-axis of the top vernier patterns.

2) Alignment of Multiple Stacked Substrates: The experimental setup is shown in Fig. 7; five 2 cm $\times$ 2 cm silicon substrates are aligned and stacked on top of each other without a placement tool. The PSAS and the inverted pyramid pits in the chips were fabricated similar to the ones described in the previous section. However, the pit and the PSAS were fabricated on the two sides of the same wafer, and the front- and back-side vernier patterns were aligned using a back-side mask alignment tool.

The alignment accuracy between the different surfaces in the stack of five substrates were also measured using an infrared microscope. By focusing on different focal planes (i.e., surfaces of substrates), it was possible to determine the misalignment at each interface. As a result, the misalignment from the back side alignment did not affect the measurement; reported are misalignment resulting from the PSAS and pit alignment technique only.

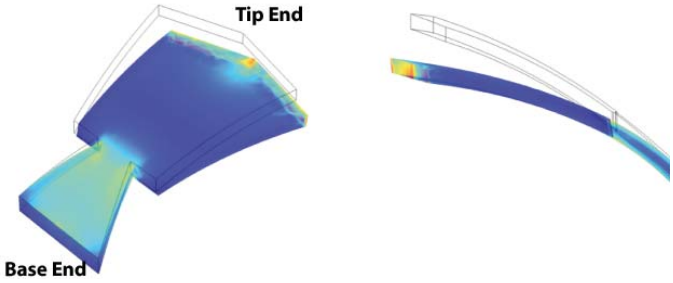

Fig. 8. Bending profile of the MFI design show that the tip remains the highest point when it is being deflected.

One challenge during the measurement was the degrading image fidelity and contrast as the microscope focused on lower surfaces of the stack; though it was possible to see the vernier patterns clearly in the first three substrates, the last two substrates were not clear enough for measurements. To obtain results for the last two surfaces, the stack was flipped upside down and measured.

The misalignments are measured at all four corners of the chip at each interface; Fig. 7 shows the average misalignment measured at each interface. The results show that alignment below 4 μm can be consistently achieved, which is slightly worse than the two-substrate case.

III. Mechanically Flexible Interconnects

MFIs are highly compliant interconnects developed to make repeatable electrical contact with various surfaces, including an FR4 surface with significant surface nonuniformity. In our previous study, we demonstrated an MFI with 65 μm gap and deflection. The shape of the interconnect is designed to maximize the vertical and elastic range of motion [14], [16]–[18]. This mechanical property enables the MFIs to deform vertically to apply pressure and to compensate for surface nonuniformity. In addition, MFIs can also move laterally, as the tip end is free to slide on the surface of the pad area. Therefore, CTE mismatch between two layers (e.g., FR4 PWB and interposer tiles) can be compensated without significant lateral deformation. Finally, in an attempt to minimize the cost, the interconnect technology was developed to be CMOS compatible and needing two photolithography steps.

MFIs used in this paper have several key improvements that are designed to address new challenges associated with temporary interconnections (Fig. 8):

1) pointy tip replaces the circular solder pad area for improved contact resistance (Fig. 9);
2) the interconnect points upward to ensure that the contact with the pad is made at the tip end (Fig. 8);
3) optimized shape ensures that the tip end remains in contact with the pad when deformed vertically while distributing the stress to maximize elastic movement range (Fig. 8).

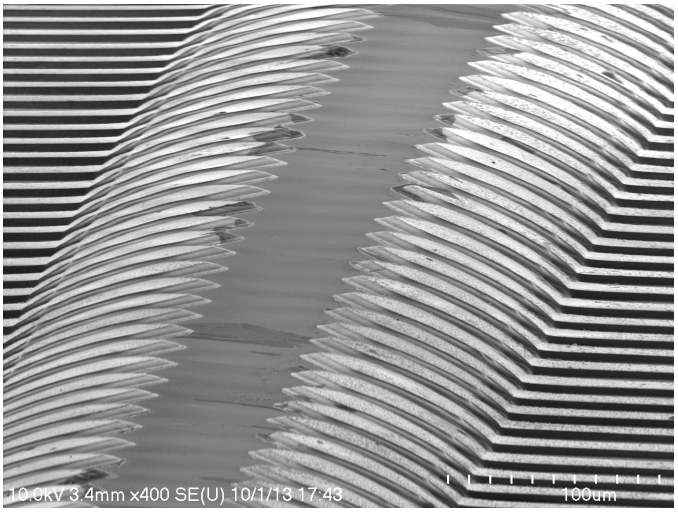

Fig. 9. SEM of MFIs showing pointy tips.

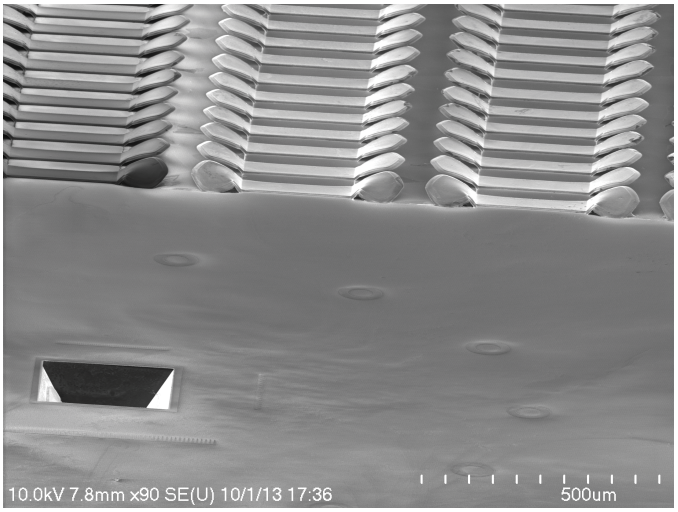

Fig. 10. MFIs are fabricated on the same surface as the inverted pyramid pits.

The MFIs are made to point upward by not using the relatively flat part of the sacrificial reflowed photoresist structure, as shown in Fig. 11. MFIs are also coated with a gold layer to improve contact resistance, and to improve lifetime as demonstrated in [17].

MFI properties are summarized in Table II. Four-point resistance measurement of a single MFI (without contact resistance) is performed by directly probing an MFI on a four-point probe station. In addition, the resistance including contact resistance is also measured using the setup shown in Fig. 12.

IV. Interposer Tiles and Silicon Bridges

In this section, interposer tiles and silicon bridges are fabricated with PSAS, inverted pyramid pits, and MFIs (Fig. 13). Three interposer tiles and two silicon bridges are aligned and assembled using PSAS and inverted pyramid pit; electrical connectivity between interposer tiles through MFIs is demonstrated. Various properties of the platform are described in Table III.

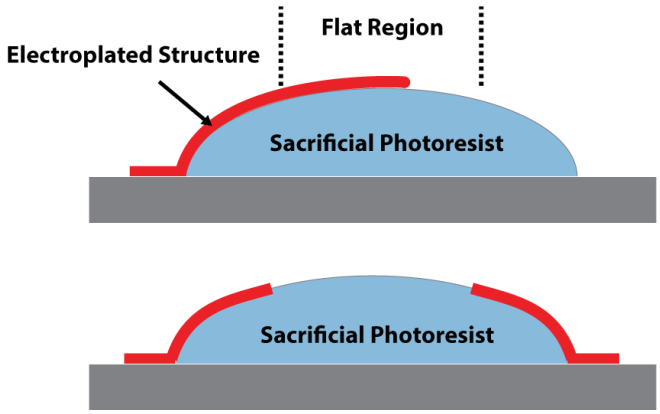

Fig. 11. MFIs point upward by not using the flat region. It is also possible to increase pitch by using both sides of the sacrificial photoresist.

TABLE II
Summary of MFI Properties

Property	Value
Material	Nickel Alloy w/ Au Coating
Pitch (μm)	X: 140 Y: 200
Initial Stand-off Height (μm)	60
MFI Thickness (μm)	7
No. of MFIs per Silicon Bridge	2000
4 Pt. R of Single MFI ($m\Omega$)	48
4 Pt. R incl. Contact R (Au Pad) ($m\Omega$)	58
4 Pt. R incl. Contact R (Al Pad) ($m\Omega$)	298

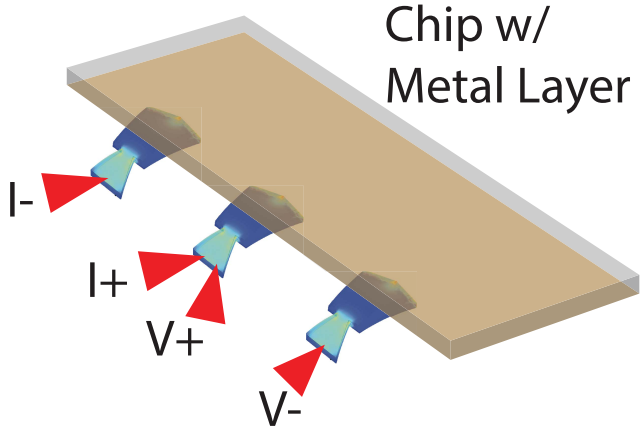

Fig. 12. Test setup for four-point resistance measurement including contact resistance. The chip is mounted using PSAS to ensure consistent contact force.

A. Interposer Tile and Silicon Bridge Fabrication

In this demonstration, interposer tiles contain inverted pyramid pits on both sides. This is because pits could not be fabricated on FR4 PWB as the pit fabrication process exploits silicon's crystalline property. This forces the PSAS to be placed on the FR4 PWB and the pits on the silicon tiles. In this paper, interposer tiles were chosen to contain MFIs and pits, however, it is also possible for silicon bridges to contain MFIs and pits (Fig. 10).

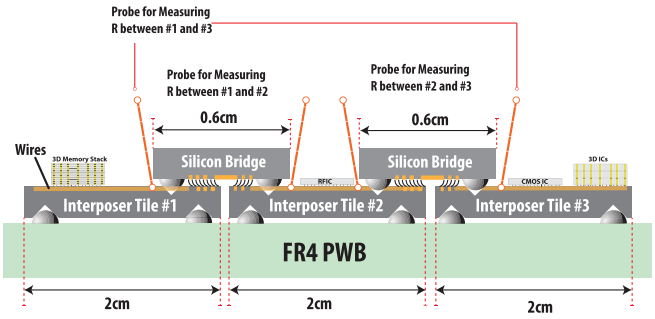

Fig. 13. Multiple interposer tiles are interconnected via MFIs and are aligned to the PWB and the silicon bridges using PSASs and pits. Probe locations for measuring the resistance between interposer tiles are identified in the figure.

TABLE III
SUMMARY OF PROPERTIES FOR ASSEMBLED PLATFORM

Property	Value
Interposer Tile Area (cm^2)	4.0
No. of Interposer Tiles	3
Silicon Bridge Area(cm^2)	1.2
No. of Silicon Bridge	2
Tile/Bridge Thickness	500 μm
Total Available Silicon Interposer Area (cm^2)	9.6

B. Assembly of Interposer Tiles and Si Bridges

After the fabrication of PSAS, pits, and MFIs, interposer tiles are brought together and coarsely aligned to the FR4 PWB. Next, interposer tiles are gently pushed downward and slightly moved around laterally until all PSAS and pit pairs engage and interposer tiles become fixed. The height of the PSAS is larger than the height of the MFIs; this prevents damage to the MFIs during the assembly process when PSAS are not completely engaged with pits and are sliding across the substrate surface. MFIs only make contact with the pad, after the PSAS have been engaged with pits and when the gap between the substrates is reduced. Silicon bridges are assembled in a similar manner. Fig. 15 shows an x-ray image of an assembled platform.

For simplicity, adhesive material is applied at the edges of the interposer tiles and the silicon bridges to hold the assembly. The assembled interposer tiles and silicon bridges are shown in Fig. 14. The measurement of the alignment accuracy before and after the application of the adhesive material shows that the alignment is not affected.

The adhesive material will be replaced with a more advanced clamping mechanism. Such clamping mechanism would enable precise control of the position as well as the magnitude of the clamping force to minimize the tile warpage and to ensure reliable operation of MFIs. The ability to clamp and unclamp the tiles and bridges in conjunction with temporary interconnects, such as MFIs, and nonbonding alignment mechanism, such as PSAS, will enable tiles and bridges to be replaced repeatedly. An example of the clamping mechanism is discussed in [19].

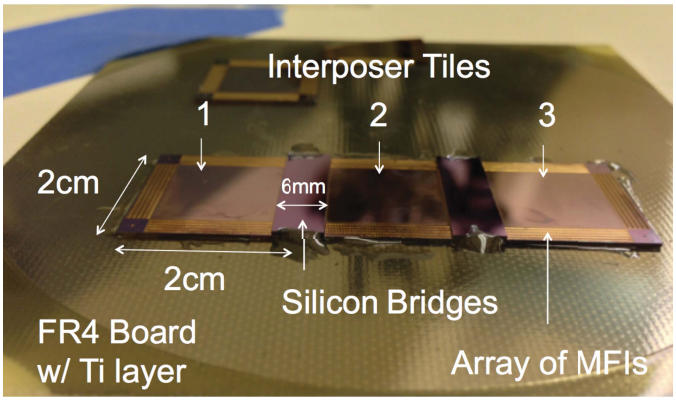

Fig. 14. Image of the three interposer tiles mounted directly on FR4 and interconnected using silicon bridges and MFIs.

TABLE IV
MISALIGNMENT BETWEEN SILICON BRIDGE AND INTERPOSER TILES

Regions	Silicon Bridge 1		Silicon Bridge 2	
	Horizontal	Vertical	Horizontal	Vertical
	(μm)		(μm)	
Bottom Left	-4.0	+4.6	-5.2	-5.0
Bottom Right	-5.4	-4.8	-5.0	-5.0
Top Right	+5.8	+3.2	-5.8	-5.2
Top Left	+6.0	-5.0	-7.6	-5.0

C. Alignment Accuracy Measurement

Accurate alignment between the interposer tiles and the silicon bridge is required in ensuring that robust interconnection is achieved for optical and electrical communication. The alignment accuracy also determines the minimum size of the interface I/Os.

Because the silicon bridges are aligned to the interposer tiles with an assumption that the interposer tiles are aligned perfectly to the PWB, it is essential that the alignment between PWB and interposer tiles are accurate even though nanophotonics and high-density I/Os do not exist between those two layers.

The alignment accuracy is measured by observing vernier patterns fabricated on the silicon bridge and the interposer tiles via infrared microscopy. Results are summarized in Table IV.

D. Electrical Measurements

Electrical resistance among interposer tiles is measured to verify electrical connectivity. Fig. 13 shows the location of the probes for measuring resistance. Table V summarizes the results. Expected values are calculated by considering the resistance of MFIs measured using four-point electrical measurement as well as the gold-coated wire traces fabricated on the interposer tiles and silicon bridges. Data shows that the resistance is within two standard deviations of the expected resistance. The major source of variation is the wire traces, which are electroless plated; noticeable thickness variation is introduced after the process.

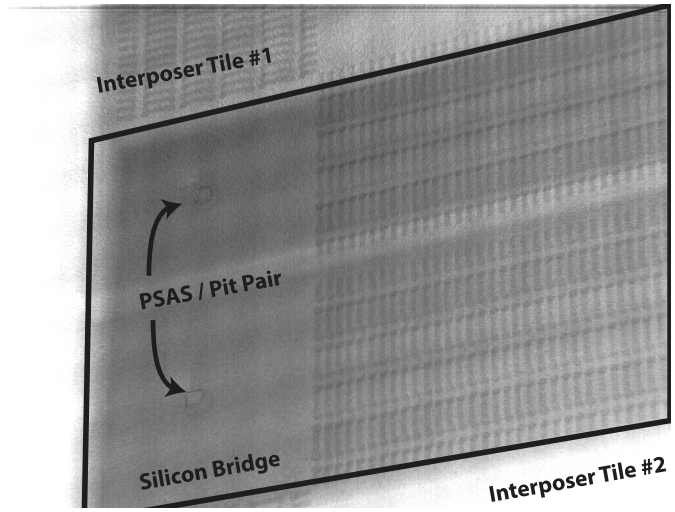

Fig. 15. X-ray image showing the two aligned pit/PSAS pair, silicon bridge, and two interposer tiles. Array of MFIs as well as traces connecting them on both the interposer tiles and the silicon bridge are shown.

TABLE V
RESISTANCE BETWEEN INTERPOSER TILES

	Resistance between interposer tiles		
	1 and 2	2 and 3	1 and 3
Average (Ω)	1.51	1.60	4.98
Expected Value (Ω)	1.32	1.32	4.36
Standard Deviation (Ω)	0.138	0.140	0.363
No. of Samples	20	20	20
No. of MFIs in Chain	20	20	40

V. CONCLUSION

In this paper, a novel large-scale silicon system platform containing multiple interposer tiles and silicon bridges is demonstrated. Accurate alignment between silicon bridges and interposer tiles makes it possible to accommodate nanophotonics to enable even higher bandwidth and lower energy in the future. Two enabling technologies are also described: 1) PSASs have been shown to align two or more substrates in various configurations consistently with 5 μm accuracy and 2) MFIs have shown electrical interconnectivity among interposer tiles and have also been shown to be compatible with the self-alignment mechanism.

The key features of the described platform are: 1) simple and accurate alignment between interposer and motherboard; 2) use of MFIs to compensate for nonplanarity and to enable rematable interposer configurations; and 3) a platform for dense electrical and photonic links between interposers without using motherboard-level interconnects.

ACKNOWLEDGMENT

The authors would like to thank H. Thacker, I. Shubin, J. Cunningham, and J. Mitchell from Oracle Labs, San Diego, CA, for valuable feedback, guidance, and support. They would also like to thank AZ Electronic Materials, Branchburg, NJ, USA, and Capitol Scientific, Inc., Austin, TX, USA, for providing the AZ 40XT-11D photoresist used to fabricate the PSASs in this paper, and R. Eakin for troubleshooting problems related to photolithography.

REFERENCES

[1] P. Dorsey, "Xilinx stacked silicon interconnect technology delivers breakthrough FPGA capacity, bandwidth, and power efficiency," Xilinx, San Jose, CA, USA, Tech. Rep. WP38, 2010.

[2] A. V. Krishnamoorthy *et al.*, "Computer systems based on silicon photonic interconnects," *Proc. IEEE*, vol. 97, no. 7, pp. 1337–1361, Jul. 2009.

[3] H. D. Thacker *et al.*, "Hybrid integration of silicon nanophotonics with 40 nm-CMOS VLSI drivers and receivers," in *Proc. IEEE 61st Electron. Compon. Technol. Conf. (ECTC)*, May/Jun. 2011, pp. 829–835.

[4] G. Li *et al.*, "Ultralow-power silicon photonic interconnect for high-performance computing systems," *Proc. SPIE*, vol. 7607, p. 760703, Feb. 2010. [Online]. Available: http://dx.doi.org/10.1117/12.842884

[5] X. Zheng *et al.*, "Ultralow power 80 Gb/s arrayed CMOS silicon photonic transceivers for WDM optical links," *J. Lightw. Technol.*, vol. 30, no. 4, pp. 641–650, Feb. 15, 2012.

[6] J. Yao *et al.*, "Grating-coupler based low-loss optical interlayer coupling," in *Proc. 8th IEEE Int. Conf. Group IV Photon. (GFP)*, Sep. 2011, pp. 383–385.

[7] A. Majumdar, J. E. Cunningham, and A. V. Krishnamoorthy, "Alignment and performance considerations for capacitive, inductive, and optical proximity communication," *IEEE Trans. Adv. Packag.*, vol. 33, no. 3, pp. 690–701, Aug. 2010.

[8] Panasonic Corporation of North America. (2012). *Panasonic BM123–133 Flyer*. [Online]. Available: http://www.panasonicfa.com/pdfs/BM123-133.pdf

[9] Panasonic Corporation of North America. (2012). *Panasonic FCB3 Flyer*. [Online]. Available: http://www.panasonicfa.com/pdfs/FCB3.pdf

[10] I. Shubin *et al.*, "A novel MCM package enabling proximity communication I-O," in *Proc. IEEE 61st Electron. Compon. Technol. Conf. (ECTC)*, May/Jun. 2011, pp. 224–229.

[11] F. Sun, Y. Leblebici, and T. Brunschwiler, "Surface-tension-driven multi-chip self-alignment techniques for heterogeneous 3D integration," in *Proc. IEEE 61st Electron. Compon. Technol. Conf. (ECTC)*, May/Jun. 2011, pp. 1153–1159.

[12] Y. Ito, T. Fukushima, K. W. Lee, K. Choki, T. Tanaka, and M. Koyanagi, "Flux-assisted self-assembly with microbump bonding for 3D heterogeneous integration," in *Proc. IEEE 63rd Electron. Compon. Technol. Conf. (ECTC)*, May 2013, pp. 891–896.

[13] K.-N. Chiang and C.-A. Yuan, "An overview of solder bump shape prediction algorithms with validations," *IEEE Trans. Adv. Packag.*, vol. 24, no. 2, pp. 158–162, May 2001.

[14] H. S. Yang and M. S. Bakir, "Design, fabrication, and characterization of freestanding mechanically flexible interconnects using curved sacrificial layer," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 2, no. 4, pp. 561–568, Apr. 2012.

[15] J. E. Cunningham *et al.*, "Integration and packaging of a macrochip with silicon nanophotonic links," *IEEE J. Sel. Topics Quantum Electron.*, vol. 17, no. 3, pp. 546–558, May/Jun. 2011.

[16] H. S. Yang and M. S. Bakir, "3D integration of CMOS and MEMS using mechanically flexible interconnects (MFI) and through silicon vias (TSV)," in *Proc. IEEE 60th Electron. Compon. Technol. Conf. (ECTC)*, Jun. 2010, pp. 822–828.

[17] C. Zhang, H. S. Yang, and M. S. Bakir, "Gold passivated mechanically flexible interconnects (MFIs) with high elastic deformation," in *Proc. IEEE 62nd Electron. Compon. Technol. Conf. (ECTC)*, May/Jun. 2012, pp. 245–250.

[18] C. Zhang, H. S. Yang, and M. S. Bakir, "Highly elastic gold passivated mechanically flexible interconnects," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 3, no. 10, pp. 1632–1639, Oct. 2013.

[19] H. S. Yang, H. D. Thacker, I. Shubin, J. E. Cunningham, and J. G. Mitchell, "Assembly and alignment of Proximity Communication enabled multi-chip packages using elastomeric bump interposers," in *Proc. IEEE 62nd Electron. Compon. Technol. Conf. (ECTC)*, May/Jun. 2012, pp. 2029–2035.

Hyung Suk Yang (S'09) received the B.S. degree in computer engineering with High Honors and the M.S. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2007 and 2008, respectively, where he is currently pursuing the Ph.D. degree in electrical and computer engineering.

His current research interests include 3-D heterogeneous integration using novel microfabricated interconnect technologies.

Mr. Yang was a recipient of the 2011–2012 Intel Corporation Ph.D. Fellowship Award.

Chaoqi Zhang (S'12) received the B.S. degree in physics from Shandong University, Jinan, China, in 2005, and the M.S. degree in microelectronics from Tsinghua University, Beijing, China, in 2008. He is currently pursuing the Ph.D. degree in electrical engineering with the Georgia Institute of Technology, Atlanta, GA, USA.

His current research interests include flexible interconnect technologies for 2.5-D/3-D heterogeneous integration.

Muhannad S. Bakir (SM'12) received the B.E.E. (*summa cum laude*) degree from Auburn University, Auburn, AL, USA, in 1999, and the M.S. and Ph.D. degrees in electrical and computer engineering from the Georgia Institute of Technology (Georgia Tech), Atlanta, GA, USA, in 2000 and 2003, respectively.

He is currently an Associate Professor and the ON Semiconductor Junior Professor with the School of Electrical and Computer Engineering, Georgia Tech.

Dr. Bakir is an Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES, an Associate Editor of the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY, and was a Guest Editor of the 2011 Special Issue of the IEEE JOURNAL OF SELECTED TOPICS IN QUANTUM ELECTRONICS. He is also a member of the International Technology Roadmap for Semiconductors technical working group for Assembly and Packaging. He was a recipient of the 2013 Intel Early Career Faculty Honor Award, the 2012 DARPA Young Faculty Award, the 2011 IEEE CPMT Society Outstanding Young Engineer Award, and was an Invited Participant in the 2012 National Academy of Engineering Frontiers of Engineering Symposium. He was also a recipient of the Semiconductor Research Corporation's Inventor Recognition Awards in 2002, 2005, and 2009. He and his research group have received 14 conference and student paper awards, including five from the IEEE Electronic Components and Technology Conference, four from the IEEE International Interconnect Technology Conference, and one from the IEEE Custom Integrated Circuits Conference.